

An Adaptive Sampling Scheme Guided by BART – With an Application to Predict Processor Performance

Abstract

The evaluation of new processor designs is an important issue in electrical and computer engineering. Architects use simulations to evaluate designs and to understand trade-offs and interactions among design parameters. However, due to the lengthy simulation time and limited resources, it is often practically impossible to simulate a full factorial design space. Effective sampling methods and predictive models are required. In this paper, we propose an automated performance predictive approach which employs an adaptive sampling scheme that interactively works with the predictive model to select samples for simulation. These samples will be used to build Bayesian additive regression trees, which are used to predict the whole design space. Both real data analysis and simulation studies show that our method is effective in that, though sampling at very few design points, it generates highly accurate predictions on the unsampled points. Furthermore, the proposed model provides quantitative interpretation tools with which investigators can efficiently tune design parameters in order to improve processor performance.

Keywords: Adaptive Design, Bayesian Additive Regression Trees, Sampling Method, Sequential G-optimization, Processor Performance.